

REMARKS

Claims 1-15 remain in the application for consideration by the examiner. The Official action set forth three different prior art rejections of applicant's claims.

Claims 1, 8, 9, and 12-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent No. 4,547,446 of Tam in view of U.S. patent No. 4,327,292 of Wang *et al.* (Wang). This rejection begins at the bottom of page 2 and continues to the middle of page 6. The teachings of Tam and Wang were newly cited against applicant's claims.

Claims 2-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tam and Wang in further view of U.S. patent No. 6,400,405 of Oishi *et al.* (Oishi). This rejection is set forth from the middle of page 6 through the top of page 7 of the Official action. On page 8, claims 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tam in view of Wang in further view of U.S. patent No. 4,418,467 of Iwai.

Applicant respectfully submits that the teachings of Tam and Wang either alone, together, or combined with the teachings of Oishi and/or Iwai do not disclose or suggest the invention as set forth in present claims 1-15 within the meaning of 35 U.S.C. § 103.

The teachings of Tam were used as a primary reference, in all of the prior art rejections and thus form the cornerstone of all the rejections against

applicant's claims. However, the teachings of Tam do not provide the disclosure for one of ordinary skill in the art as alleged in the outstanding Office action. In particular, the teachings of Tam never state that marks are provided on a peripheral edge of the wafer as required in applicant's claims. Since the teachings of Tam are deficient for suggesting the basic structure of applicant's claimed invention, all the rejections of applicant's claims which rely on Tam as a primary reference, cannot establish a *prima facie* case of obviousness for the presently claimed invention.

In particular, the Official action noted Fig. 3 of Tam as disclosing a semiconductor wafer 36 having an outer peripheral face containing a notch (at the place of 38) having an inner wall face extending inwardly and away from the outer peripheral face of the semiconductor wafer towards the center of the semiconductor, where markings (38) are formed on the inner wall surface. However, Tam does not teach this. The teachings of Tam never disclose or suggest that the wafer therein has markings on the peripheral surface of the notch. Items 38 and 20 shown in Fig. 3 of Tam are not part of the wafer 36. These items are part of the universal master mask 10 as shown in Fig. 1, which is discussed at column 4, lines 21-33, of Tam. For purposes of aligning the wafer, the mask 10 is provided with alignment patterns 38 and 20, and the edge of the wafer is aligned to intersect the center points of the alignment patterns 38 and 20 (of the mask 10).

The specification of Tam never describes that the wafer is provided with markings on its peripheral edge, especially on an inner wall face of a notch, as required in the present claims. It appears that Fig. 3 of Wang simply shows the alignment patterns 38 and 20 of the mask together with the wafer 36.

Since the teachings of Tam do not contemplate or suggest a semiconductor wafer having an outer peripheral face containing a notch having an inner wall face extending inwardly and away from the outer peripheral face of the semiconductor wafer towards a center of the semiconductor wafer, wherein markings are formed on the inner wall face, and no other teachings have been cited as suggesting this structure of applicant's claimed invention, all the rejections against applicant's claims must fail. Therefore, applicant respectfully requests that the examiner reconsider and withdraw all the rejections as set forth in the outstanding Office action.

It is respectfully noted that the Official action sets forth some comments concerning the limitations in applicant's claims as product-by-process language. Applicant is not requesting that the examiner make any determination or consideration that is not in accordance with all the case law cited in the outstanding Office action. In patent claims, structure can be defined by the process in which it is made. For example, a clean dish has a structure that is different from a dish soiled with food, and a frosted glass has a structure different from a non-frosted glass. Along these same lines, the process limitation set forth in applicant's claims define a semiconductor wafer

having a specific structure. Considering applicant's claims, it is respectfully noted that applicant's claim 12 defines when the markings are arranged on the inner surface of the notch prior to various fabrication steps. For example, this claim defines the semiconductor at a point in time, mainly, before fabrication, when the markings were provided on the semiconductor. In order for the prior art to render such a claim obvious, prior art would have to show a semiconductor wafer that had or has markings on the inner surface of the notch before processing of the semiconductor wafer. If such a semiconductor wafer was subjected to later fabrication steps, the appearance of the markings will change due to such fabrication steps. The applicant cannot find such structure in the teachings of the cited prior art.

Applicant's claim 13 defines that the markings contained all the history information concerning the fabrication steps for fabricating the semiconductor wafer. This claim defines the information contained in the markings identifies all the fabrication steps used when fabricating the wafer. Applicant cannot find any discussion in the cited teachings concerning this aspect of the presently claimed invention.

Applicant's claim 14 defines a marked semiconductor made from a semiconductor wafer that was subjected to at least one fabrication step that is visibly discernable on the marked semiconductor wafer. This claim defines a semiconductor that was marked prior to at least one fabrication step at a time, after the fabrication step(s) were completed, and requires that the markings are

still present. In other words, this claim defines a wafer having markings thereon that have survived fabrication step(s). The applicant cannot find this structure in the prior art cited in the outstanding Office action.

Claim 15 includes language similar to that of claim 14. Claim 15 defines that the peripheral surface of the semiconductor wafer contains visibly discernable structure resulting from processing steps. Such processing steps can include cleaning, polishing, slicing, etc. There is a difference in structure between a cleaned and an uncleaned wafer, a polished and an unpolished wafer, and a sliced and an unsliced wafer; the same difference as there is a difference between a clean plate and a plate soiled with food. Thus, these limitations in applicant's claims concerning visibly discernible structure resulting from processing steps define physical limitations that can be observed visually and/or touched. These are the limitations that the applicant found necessary to properly define the present invention. Since the cited prior art does not show these limitations, the cited prior art cannot establish a *prima facie* case of obviousness against applicant's claims within the meaning of 35 U.S.C. §103. Therefore, applicant respectfully requests that the examiner reconsider and withdraw all the rejections of the present claims.

The teachings of Oishi and Iwai do not cure or rectify the aforementioned deficiencies in the teachings of Tam and Wang. The teachings of Oishi and Iwai were discussed and distinguished from applicant's claimed

invention in the previous response filed on March 31, 2003, which comments are incorporated herein by reference.

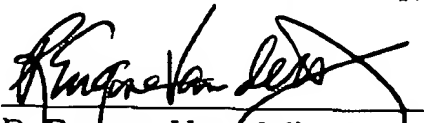
For the foregoing reasons, applicant respectfully submits that none of the teachings of Tam, Wang, Iwai, and Oishi, either taken alone or in combination, contemplate or suggest the invention as set forth in any of the present claims within the meanings of 35 USC § 102 or 35 USC § 103. Therefore, applicant respectfully requests that the examiner reconsider and withdraw all the prior art rejections of applicant's claims in the outstanding Office action

In view of the foregoing amendments and remarks, applicant respectfully submits that claims 1-15 are in condition for allowance. Accordingly, a formal allowance of these claims is respectfully requested.

The foregoing is believed to be a complete and proper response to the Official action mailed June 11, 2003. While it is believed that all the claims in this application are in condition for allowance, should the examiner have any comments or questions, it is respectfully requested that the undersigned be telephoned at the below listed number to resolve any outstanding issues.

In the event this paper is not timely filed, applicant hereby petitions for an appropriate extension of time. The fee therefor, as well as any other fees which become due, may be charged to our deposit account No. 22-0256.

Respectfully submitted,
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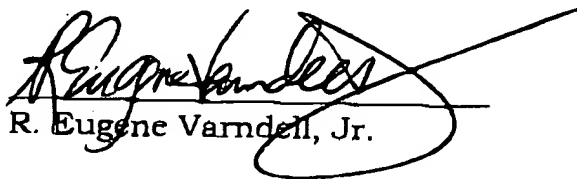
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C rtification of Transmissi n

I hereby certify that this correspondence including a Response After Final under 37 C.F.R. § 1.116 in U.S. Serial No. 09/492,761 (by Teichirou Chiba *et al.*, filed January 27, 2000), which totals 9 pages including this certification, is being facsimile transmitted to the Patent and Trademark Office (Fax No. 703-308-7722) on September 11, 2003.


R. Eugene Varndell, Jr.

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